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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,276	03/24/2004	Kouji Takezoe	2004-0454A	4006

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EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,276	TAKEZOE ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/24/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 14-16, 23 and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Toshiaki (JP 2002-076101).

2. Regarding claim 1, Toshiaki discloses a method for manufacturing semiconductor chip that a semiconductor wafer, having a surface segmented by streets and formed with a plurality of circuits, is divided into individual circuit-based semiconductor chips, the method comprising: a support substrate integration step of bonding a surface of a semiconductor wafer to a light-transmissive support substrate through an adhesive layer having an adhesion force to reduce upon exposed to light radiation, thereby exposing a back surface of the semiconductor wafer (0007-0008); a grinding step of resting the semiconductor wafer integrated with the support substrate on a chuck table of a grinding device and grinding a back surface of the semiconductor wafer (0011-0012); a tape bonding step of bonding a tape on the back surface of the semiconductor wafer integrated with the support substrate after the grinding step, while bonding a frame on a periphery of the tape (0012); a re-bonding step of applying light radiation

to the adhesive layer from a side of the support substrate before or after the tape bonding step to thereby reduce the adhesion force of the adhesive layer, and removing the support substrate and adhesive layer from the surface of the semiconductor wafer after the tape bonding step to thereby support the semiconductor wafer by the tape and a frame (0012); and a dicing step of resting the semiconductor wafer supported by the tape and frame on a chuck table of a dicing apparatus and cutting along the streets segmenting for a plurality of circuits into individual semiconductor chips (0026).

3. Regarding claim 2, Toshiaki discloses a method for manufacturing semiconductor chip that a semiconductor wafer, having a surface segmented by streets and formed with a plurality of circuits, is divided into individual circuit-based semiconductor chips, the method comprising: a groove forming step of resting a semiconductor wafer on a chuck table of a dicing apparatus and forming grooves on street surface segmenting for a plurality of circuits (0018); a support substrate integrating step of bonding a surface of the semiconductor wafer to a light-transmissive support substrate through an adhesive layer having an adhesion force to reduce upon exposed to light radiation, thereby exposing a back surface of the semiconductor wafer (0007-0012); a grinding step of resting the semiconductor wafer integrated with the support substrate on a chuck table of a grinding apparatus and grinding the back surface of the semiconductor wafer into individual semiconductor chips until the grooves are surfaced (0012); a tape bonding step of bonding a tape on the back surface of the semiconductor chip in a state integrated with the support substrate of after grinding step and maintaining an outer shape of the semiconductor wafer, and supporting a periphery of the tape by a frame (0012); and a re-bonding step of applying light radiation to the adhesive layer at a side close to the support substrate

before or after the tape bonding step to thereby reduce an adhesion force of the adhesive layer, and removing the supporting substrate and adhesive layer from the surface of the semiconductor wafer after the tape bonding step thereby supporting the semiconductor wafer by the tape and frame (0012).

4. Regarding claim 3, Toshiaki discloses a method for manufacturing semiconductor chip that semiconductor wafer, having a surface segmented by streets and formed with a plurality of circuits, is divided into individual circuit-based semiconductor chips, the method comprising: a groove forming step of resting a semiconductor wafer on a chuck table of a dicing apparatus and forming grooves on street surface segmenting for a plurality of circuits (0018); a support substrate integrating step of bonding a surface of the semiconductor wafer to a light-transmissive support substrate through an adhesive layer having an adhesion force to reduce upon exposed to light radiation, thereby exposing a back surface of the semiconductor wafer (0007-0012); a grinding step of resting the semiconductor wafer integrated with the support substrate on a chuck table of a grinding apparatus and grinding the back surface of the semiconductor wafer into individual semiconductor chips until the grooves are surfaced (0012); and a semiconductor chip detaching step of applying light radiation to the adhesive layer at a side close to the support substrate to thereby reduce an adhesion force thereof, and removing semiconductor chips from the support substrate and adhesive layer (Drawing 7).

5. Regarding claim 4, Toshiaki wherein the support substrate integrating step is carried out using the support substrate having an outer shape greater than an outer shape of the semiconductor wafer, the grinding step being carried out while measuring a thickness of the semiconductor wafer by contacting probes of a thickness measuring instrument respectively with

a grinding surface of the semiconductor wafer and with a surface of the support substrate (0020-0026).

6. Regarding claim 14, Toshiaki discloses wherein the support substrate is formed by a transparent plate of glass or plastic having a thickness of 0.5 - 2.5mm (Drawing 1, reference 11).

7. Regarding claim 15, Toshiaki wherein the support substrate integrating step is carried out using the support substrate having an outer shape greater than an outer shape of the semiconductor wafer, the grinding step being carried out while measuring a thickness of the semiconductor wafer by contacting probes of a thickness measuring instrument respectively with a grinding surface of the semiconductor wafer and with a surface of the support substrate (0020-0026).

8. Regarding claim 16, Toshiaki wherein the support substrate integrating step is carried out using the support substrate having an outer shape greater than an outer shape of the semiconductor wafer, the grinding step being carried out while measuring a thickness of the semiconductor wafer by contacting probes of a thickness measuring instrument respectively with a grinding surface of the semiconductor wafer and with a surface of the support substrate (0020-0026).

9. Regarding claim 23, Toshiaki discloses wherein the support substrate is formed by a transparent plate of glass or plastic having a thickness of 0.5 - 2.5mm (Drawing 1, reference 11).

10. Regarding claim 24, Toshiaki discloses wherein the support substrate is formed by a transparent plate of glass or plastic having a thickness of 0.5 - 2.5mm (Drawing 1, reference 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-11, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshiaka (JP 2002-076101) in view of Nikura et al (5,518,860).

11. Toshiaka discloses all above subject matter except the adhesive layer being a liquid resin containing quinone-diazido (claims 5-7), the quinone-diazido being an acid (claims 8, 17 and 18) nor the resin being selected from acryl, urethane, polyester or novolak phenol (claims 9-11).

Nikura et al discloses the adhesive layer being a liquid resin containing quinone-diazido (column 1, lines 42-49), the quinone-diazido being an acid (column 3, lines 52-67 thru column 4, lines 1-7) and the resin being selected from acryl, urethane, polyester or novolak phenol (column 3, lines 52-67 thru column 4, lines 1-7).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Toshiaka with the teachings of Nikura et al for the purpose of creating a positive working photoresist composition comprising novolac resin as the film forming agent and a

quinonediazido group containing compound as the photosensitizing agent in order to improve the adhesive bonding of the resist layer to the substrate.

Claims 12, 13 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshiaka (JP 2002-076101) in view of Misumi et al (6,641,972 B2).

12. Toshiaka discloses all above independent claimed subject matter except the liquid resin having a viscosity of 10-100000mPa s (claims 12, 19 and 20) and wherein in the support substrate integrating step, the liquid resin is dripped on the surface of the support substrate or the semiconductor wafer and spin-coated under rotation at 100-8000 rpm for 5 seconds or more, and thereafter the semiconductor wafer and the support substrate are united together through the liquid resin and baked at 50-150C for 30 seconds to 20 minutes (claims 13, 21 and 22).

Misumi et al discloses the liquid resin having a viscosity of 10-100000mPa s (column 10, lines 36-68) and wherein in the support substrate integrating step, the liquid resin is dripped on the surface of the support substrate or the semiconductor wafer and spin-coated under rotation at 100-8000 rpm for 5 seconds or more, and thereafter the semiconductor wafer and the support substrate are united together through the liquid resin and baked at 50-150C for 30 seconds to 20 minutes (column 11, lines 6-19).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Toshiaka with the teachings of Misumi et al for the purpose of creating a positive photoresist composition that is applied onto a substrate on an electronic part, patterned, plated and thereby yields bumps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
January 6, 2006

LAURA M. SCHILLINGER
PRIMARY EXAMINER